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CLEAN VERSION OF PENDING CLAIMS

METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT
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Serial No.: 09/382,442

Claims 1-2, 4-14, 26-32 and 35-39, as of May 21, 2002 (Date of Response to Final Office Action filed)

1. A method for reducing random single bit data loss in a FLASH memory circuit comprising:

providing a semiconductor layer having a surface;

heating the layer in an atmosphere comprising a Hydrogen isotope; and

fabricating a memory circuit comprising single bit data using the semiconductor layer wherein single bit data loss is reduced.

2. The method of claim 1 and further comprising forming a film on the semiconductor layer that comprises the Hydrogen isotope.

4. The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that oxidizes the semiconductor layer.

5. The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that anneals the semiconductor layer.

6. The method of claim 1 and further comprising exposing the semiconductor layer, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature.

7. The method of claim 1 and further comprising fabricating a gate region within the memory circuit.

8. The method of claim 7 and further comprising forming a film comprising Hydrogen isotope adjacent to the gate region of the memory circuit in order to reduce single bit data loss.

9. The method of claim 7 and further comprising forming a film comprising Hydrogen isotope within the gate region of the memory circuit in order to reduce single bit data loss.

10. The method of claim 1 and further comprising passivating the semiconductor layer in an atmosphere comprising Hydrogen isotope.

11. The method of claim 1 and further comprising forming a field oxide in the semiconductor layer.

12. The method of claim 11 and further comprising annealing the field oxide layer in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound.

13. The method of claim 11 and further comprising annealing at a temperature that is at least about 800 degrees Centigrade.

14. The method of claim 11 and further comprising oxidizing the annealed field oxide layer in an atmosphere that comprises Hydrogen isotope.

26. A method of forming a non-volatile electrically alterable semiconductor memory cell with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

growing an oxide over the channel region in an atmosphere

enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell comprising single bit data in an atmosphere that comprises

Hydrogen isotope thereby reducing single bit data loss.

27. The method of claim 26 and further including nitridizing the field oxide region by annealing in an atmosphere comprising Hydrogen isotope or a compound that comprises Hydrogen isotope.

28. The method of claim 26 and further comprising nitridizing at a temperature that is greater than or equal to about 800 degrees Centigrade.

29. The method of claim 26 and further including oxidizing the nitridized field layer in an atmosphere that comprises Hydrogen isotope.

30. The method of claim 26 and further comprising introducing the Hydrogen isotope by thermal oxidation.

31. The method of claim 26 and further comprising introducing the Hydrogen isotope by pyrolytic diffusion of Hydrogen isotope into the memory cell.

32. The method of claim 26 and further comprising introducing the Hydrogen isotope by RF sputter deposition.

35. A method for passivating a non-volatile, electrically alterable semiconductor memory cell, thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a non-volatile, electrically alterable semiconductor memory cell comprising single bit data; and

exposing the memory cell to an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss.

36. The method of claim 35 and further including heating the atmosphere.

37. A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a silicon substrate and providing a memory cell comprising single bit data;

defining source and drain regions in the silicon substrate; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss in the memory cell.

38. The method of claim 37 and further comprising heating the atmosphere that comprises Hydrogen isotope.

39. The method of claim 37 and further comprising defining the source and drain regions by targeted Hydrogen isotope implantation.